Sheet 1 of 2 Docket Number 188122000700 Application Number 10/773,541 Form PTO-1449 Applicant INFORMATION BISCL **E CITATION** Yutao MA et al. IN AN APPLICATION Group Art Unit 2825 Filing Date February 6, 2004 (Use several sheets if necessary) Mailing Date June 1, 2004 **U.S. PATENT DOCUMENTS** Class Subclass Filing Date If Document No. Name Examiner Ref. Date Appropriate Initials No. FOREIGN PATENT DOCUMENTS Date Class Subclass Translation Examiner Ref. Document No. Country YES NO Initials No. OTHER DOCUMENTS (including author, title, Date, Pertinent Pages, Etc.) Title Examiner Ref. **Initials** No. Achar, R. et al., (May 2001). "Simulation of High-Speed Interconnects," Proceeding of the IEEE 89(5):693-728. Bomhof, C. W. (2001). "Introduction," Chapter 1 In Interative and Parallel Methods for Linear 2. Systems, With Applications in Circuit Simulation, located at http://www.library.uu.nl/digiarchief/dip/diss/1957853/c1.pdf, last visited on June 15, 2004, 15 pages (Includes Table of Contents). Devgan, A. (1995) "Efficient and Accurate Transient Simulation in Charge-Voltage Plane," 3. International Conference on Computer Aided Design (ICCAD '95) Proceedings of the 1995 ガ IEEE/ACM international conference on Computer-aided design, San Jose, California, United States, Pages: 110 - 114. Nguyen, T. V. et al., (1998). "Simulation of Coupling Capacitances Using Matrix Partitioning," 4. International Conference on Computer Aided Design (ICCAD '98), Proceedings of the 1998 \mathcal{T} IEEE/ACM international conference on Computer-aided design, San Jose, California, United States Pages: 12 - 18. Schwarz, D. E. et al., (2000). "Structural Analysis For Electric Circuits and Consequences for MNA," 5. TT Int. J. Circ. Theor. Appl. 28:131-162. Krummenacher, F. et al., (July 28, 2000). "RF EKV MOSFET Model Implementation," EPFL -6. Electronics Laboratories (LEG), EPF-Lausanne, Switzerland, Craft European Project No. 25710, July 28, 2000, WP2, Deliverable D2.1, Ecole Polytechnique Federale de Lausanne 4 pages. Zhou, X. (2000). "Multi-Level Modeling of Deep-Submicron Mosfets and ULSI Circuits," 9th 7. International Conference on Mixed Design of Integrated Circuits and Systems, Mixdes 2002, DATE CONSIDERED: 06/06/ **EXAMINER:** 2006 EXAMINER: Initial if citation considered, whether or not the citation conforms with MPEP 609. Draw a line through the citation if not in conformance and not considered. Include a copy of this form with next communication to applicant.

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

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Applicant	

Yutao MA et al.

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Wroclaw, Poland, June 20-22, 2002, 7 pages. (NUT CONSIDERED BECAUSE

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